UM0131
USER MANUAL

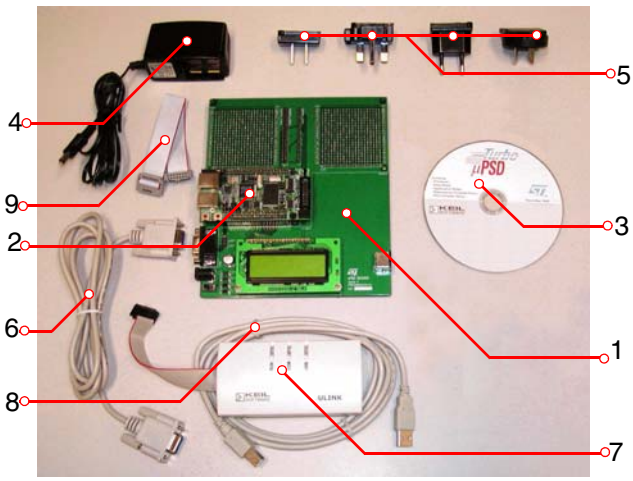
Turbo Plus uPSD DK3400 Development Kit

1 Introduction

To enhance the feature set of uPSD Turbo Family, the USB Microcontroller Development Kit DK3400 has been released from STMicroelectronics. The kit is a demo board for the uPSD3400 family which is a series of 8051 class microcontrollers (MCUs) that contain a fast Turbo Plus 8032 core with 16-bit code fetch path, full-speed USB port, a large Dual Bank Flash memory, a large SRAM, many peripherals, programmable logic and a JTAG Debug / In System Programming (ISP) port. The DK3400 kit consists of an ED3K4 module and DK3400 motherboard as well as all the items needed to explore the uPSD3400 MCU. There are also demonstration application examples along with an evaluation copy of the tools needed to develop and compile code for the uPSD3400.

Figure 1. DK3400 Contents

1. DK3400 Motherboard
2. ED3K4 uPSD3400 module
3. DK3400 CD
4. 110V/220V AC adapter
5. Plug adapters
6. RS232 Serial Cable
7. USB ULINK Adapter
8. USB Cables (x2, only 1 shown): 1 for ULINK, 1 for uPSD
9. 14-pin female-female ribbon cable (JTAG)
10. Quick Start Flyer (not shown)



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2 DK3400 Hardware Features

The DK3400 comprises both the ED3K4 board and DK3400 motherboard. ED3K4 is able to work as an uPSD3400 module independently or work together with DK3400 motherboard. The DK3400 motherboard works as a base board for the ED3K4. It is possible to upgrade the motherboard with extension boards (for example, ED3K3 and DKMMX which are currently in development).

The DK3400 motherboard itself has a variety of hardware capabilities built-in. A number of hardware features on the DK3400 are provided to enable exploration by the user and for future demo application software, including (see *Figure 2* and *Figure 3*):

- Two selectable power sources of ED3K4: USB cable and 5V wall adapter
- Dual USB port for E-RLINK and uPSD USB users respectively
- Total of 100 pins for extension connector
- One JTAG port
- One RS232 connector
- One small regulated 5V power jack on ED3K4 and one 9V power jack on the DK3400 motherboard
- 128 Mbit NAND Flash
- Very small QFN package RTC from STMicroelectronics
- 8 Mbit SPI interface Flash
- 16 Kbit I2C interface EEPROM
- Embedded debug tools RLINK
- IrDA transceiver
- 122*32 Dot Matrix LCD with Chinese font support
- PS/2 standard keyboard connector

Figure 2. ED3K4 Board Features

1. USB port for E-RLINK
2. USB port for uPSD user
3. Power-on Switch
4. Reset Switch
5. 5V power jack
6. 14-pin JTAG Connector
7. uPSD34XX
8. Expansion Connectors
9. IrDA Transceiver
10. NAND flash
11. Real-Time Clock
12. I2C interface EEPROM
13. SPI interface Flash
14. RS232 transceiver
15. Power management

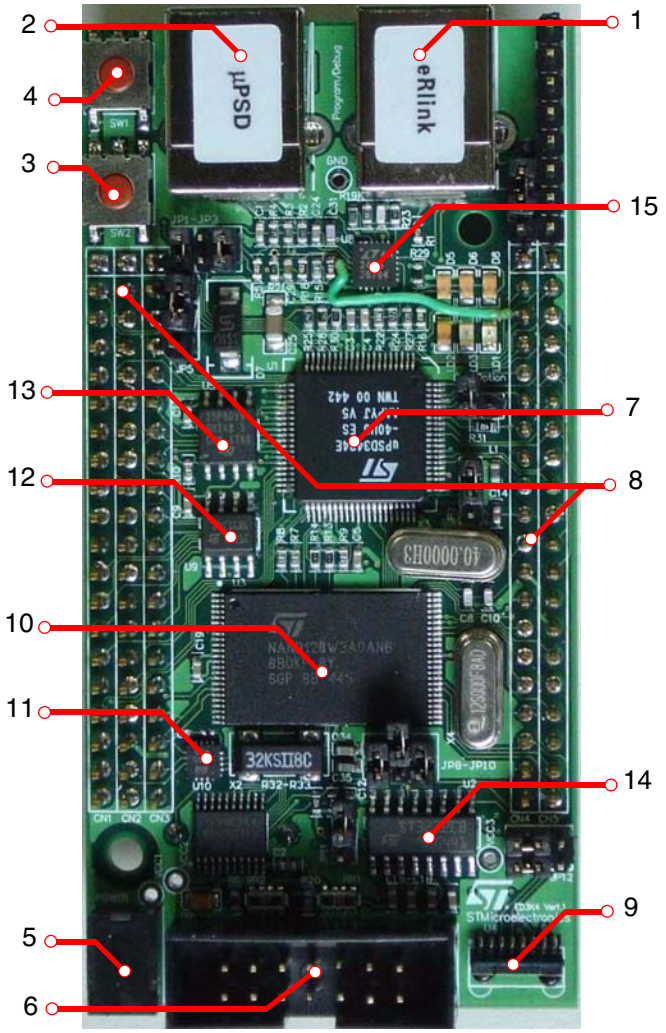
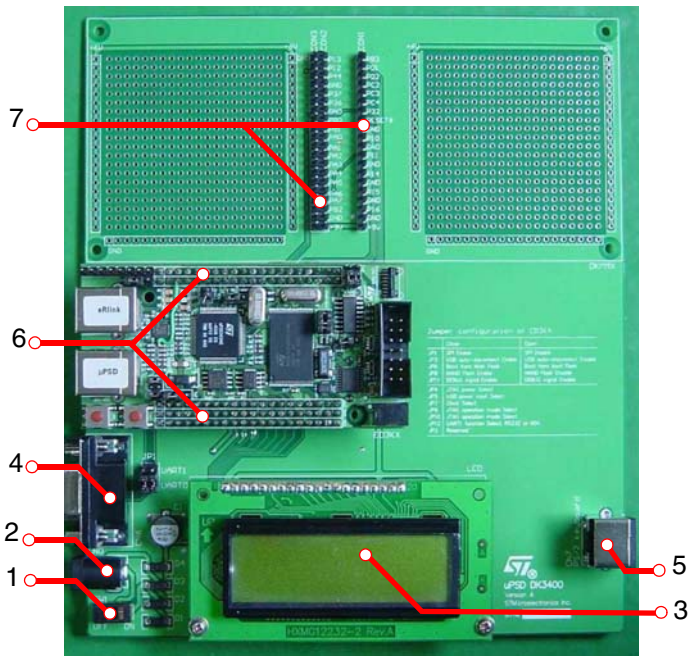


Figure 3. DK3400 Motherboard Features

1. Power Switch
2. 9V Power Input
3. Dot Matrix LCD
4. RS232 connector
5. PS/2 connector
6. Connectors for ED3Kx
7. Connectors for DKMMX



3 ED3K4 Hardware and Operation Mode

The ED3K4 is a very low cost uPSD3400 evaluation module with full-speed USB support, embedded debug tools RLINK and 128-Mbit NAND flash. Depending on different application purposes, ED3K4 can be configured to one of the following 5 operation modes:

- Mode1: USB mass storage mode
- Mode2: uPSD3400+E-RLINK mode
- Mode3: Stand-alone RLINK mode
- Mode4: uPSD3400+ULINK mode
- Mode5: ED3K4+DK3400 motherboard mode

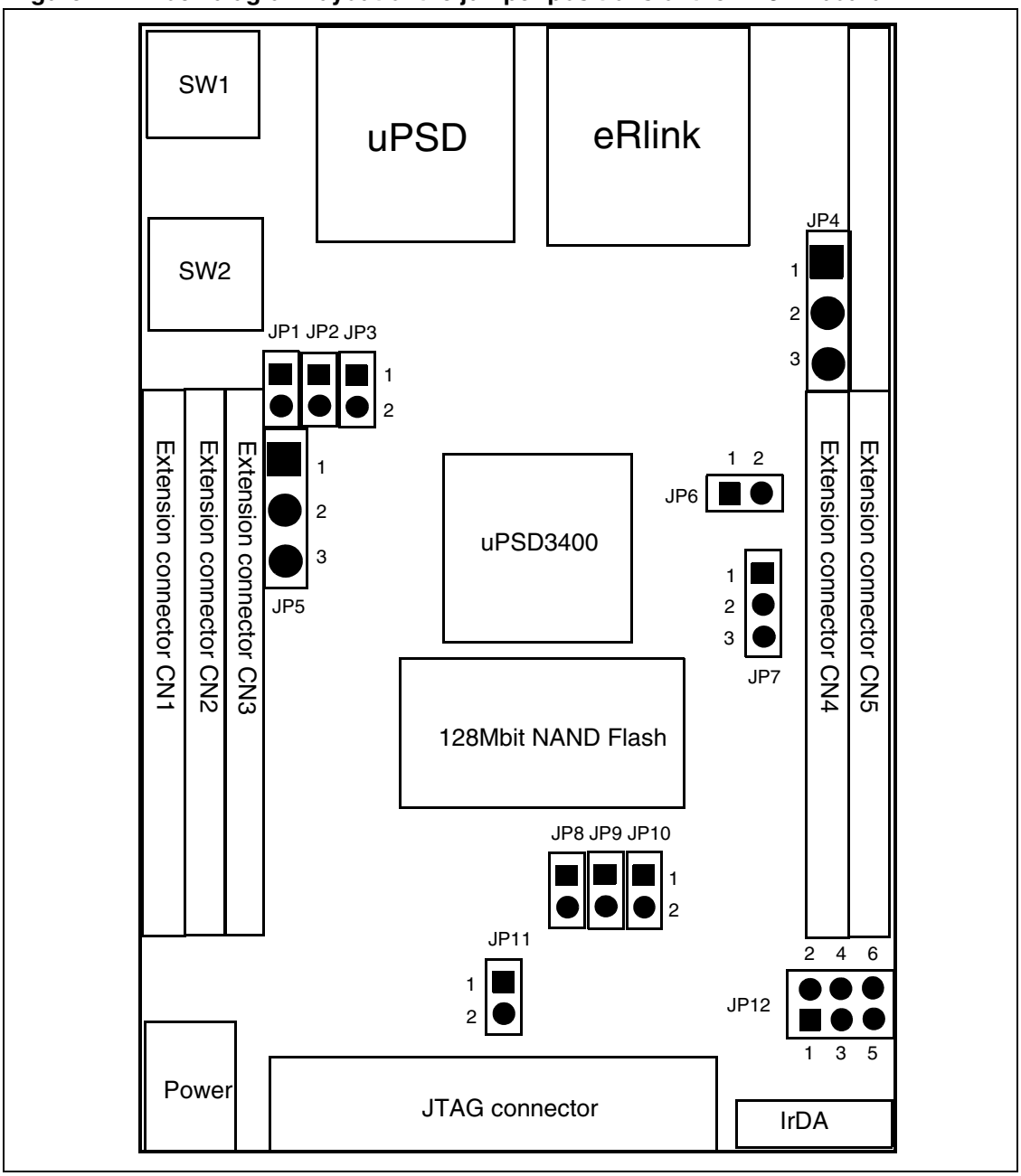
The 5 operation modes will be introduced in detail later.

3.1 ED3K4 Hardware Architecture

The jumpers and connectors definitions on ED3K4 board are detailed in this chapter.

3.1.1 ED3K4 Jumpers Diagram

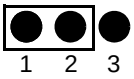
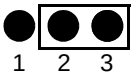
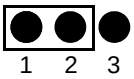
Figure 4. Block diagram layout of the jumper positions of the ED3K4 board

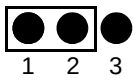
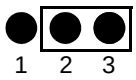
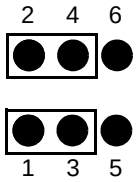
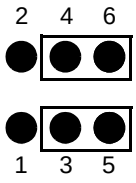


3.1.2 Jumpers Description

The definitions of the jumpers on ED3K4 board are listed in *Table 1*:

Table 1. Description of jumpers on ED3K4 board

Jumper	Description
JP1	JP1 is used to enable SPI interface Flash M25P80. M25P80 is enabled when JP1 is closed. Default status: closed
JP2	Reserved. Please keep this jumper on open. Default status: open
JP3	JP3 is used to enable USB auto-disconnect function. USB auto-disconnect function is enabled when JP3 is closed. Default status: closed
JP4	JP4 is used to select a power source for JTAG port. Keep JP4 on following status when ED3K4 works on Mode1, 2, 4 and 5:  Keep JP4 on open when ED3K4 works on Mode 3. Default status: JP4.1 connected to JP4.2
JP5	JP5 is used to select which power source will be used as USB power input of power management circuit, power from E-RLINK USB cable or power from uPSD USB cable. Keep JP5 on following status when ED3K4 powered from RLINK USB cable:  Keep JP5 on following status when ED3K4 powered from uPSD USB cable:  Default status: JP5.1 connected to JP5.2
JP6	JP6 is used to provide a boot option for ED3K4 board. ED3K4 boot from internal main flash when JP6 is closed. ED3K4 boot from internal boot flash when JP6 is open. Default status: open

JP7	JP7 is used to select clock generation source, external clock or internal clock. ED3K4 works with internal clock when JP7 is set as following:  ED3K4 works on external clock mode when JP4 is set as following:  Default status: JP7.1 connected to JP7.2
JP8	JP8 is used to enable NAND Flash. 128Mbit NAND flash is enabled when JP8 is closed. Default status: closed
JP9	JP9 is used to select JTAG circuit operation mode along with JP10 depending on operation mode of ED3K4. Keeps JP9 on closed when ED3K4 works on mode 1, 2, 3 and 5. Keeps JP9 on open when ED3K4 works on mode 4. Default status: closed
JP10	JP10 is used to select JTAG circuit operation mode along with JP9 depending on operation mode of ED3K4. Keeps JP10 on closed when ED3K4 works on mode 1, 2, 4 and 5. Keeps JP10 on open when ED3K4 works on mode 3. Default status: closed
JP11	JP11 is used to enable DEBUG signal. DEBUG signal is enabled when JP11 is closed. Default status: open
JP12	JP12 is used to select which transceiver will be connected to UART1 port, RS232 transceiver or IrDA transceiver. UART1 is connected to RS232 transceiver when JP12 is set as following:  UART1 is connected to IrDA transceiver when JP12 is set as following:  Default status JP12.2 connected to JP12.4; Default status JP12.1 connected to JP12.3.

3.1.3 Connector Description

The definitions of connectors on ED3K4 board are listed in *Table 2* and *Table 3*:

Table 2. Description of connectors on ED3K4 board

Connector	Description
POWER	Regulated 5V power jack. **Note:** The absolute Maximum voltage on this jack is 6V.
USER USB	USB port connected to uPSD3400 on board.
E-RLINK USB	USB port for embedded RLINK
JTAG	JTAG port used for debugging and programming
CN1, 2, 3, 4 and 5	100 pins Extension connectors for user.

Table 3. Description of the 100-pin extension connector CN1,2,3,4 and 5

Connector	Signal Name	Pins	Description
CN1	RD#	1	READ signal
	WR#	2	WRITE signal
	GND	3,4,5,6,7,8 9,10,11	Ground
	MCU_AD0	12	Multiplexed Address/Data bus A0/D0
	MCU_AD1	13	Multiplexed Address/Data bus A1/D1
	MCU_AD2	14	Multiplexed Address/Data bus A2/D2
	MCU_AD3	15	Multiplexed Address/Data bus A3/D3
	MCU_AD4	16	Multiplexed Address/Data bus A4/D4
	MCU_AD5	17	Multiplexed Address/Data bus A5/D5
	MCU_AD6	18	Multiplexed Address/Data bus A6/D6
	MCU_AD7	19	Multiplexed Address/Data bus A7/D7
	PSEN#	20	PSEN signal external bus
CN2	PC2/VSTBY	1	GPIO/PLD Output or Input/SRAM standby voltage input(Vstby)
	GND	2,19	Ground
	VCC1	3,4,5,6,7,8	External 5V wall adapter power source (5-6V)
	PA7	9	GPIO on port A
	PA6	10	GPIO on port A
	PA5	11	GPIO on port A
	PA4	12	GPIO on port A
	PWR_DOWN	13,17	Reserved
	PA3	14	GPIO on port A
	PA2	15	GPIO on port A
	P34/C0	16	GPIO/Counter 0 input
	VBATT	18	Reserved
	EXT_CLK	20	External clock input

CN3	PC3/TSTAT	1	GPIO/optional JTAG status(TSTAT)
	MCU_SPI_SEL	2	SPI slave select signal
	MCU_SPI_TXD	3	SPI TXD signal
	MCU_SPI_RXD	4	SPI RXD signal
	MCU_SPI_CLK	5	SPI clock signal output
	P42/TCM2	6	GPIO/PCA0-TCM2/UART1 RXD signal
	P41/TCM1	7	GPIO/PCA0-TCM1/Timer 2 trigger input
	P40/TCM0	8	GPIO/PCA0-TCM0/Timer 2 counter input
	P32/INT0	9	GPIO/External interrupt0 input
	P33/INT1	10	GPIO/External interrupt1 input
	P11/T2X	11	GPIO/Timer 2 trigger input/ADC channel 1
	GND	12,17	Ground
	TXD1_232	13	UART1 TXD signal on RS232 voltage level
	RXD1_232	14	UART1 RXD signal on RS232 voltage level
	PA1	15	GPIO on port A
	PA0	16	GPIO on port A
	P36/SDA	18	GPIO/I2C Bus serial data
	P37/SCL	19	GPIO/I2C Bus clock
	VCC3	20	3.3V power
CN4	CPU_DEBUG	1	I/O to the MCU Debug Unit
	PC7	2	GPIO/PLD input and output
	PD1	3	GPIO/PLD IO
	PB0	4	GPIO/PLD IO/Address Latch output
	P31/TXD0	5	GPIO/UART0 transmit TXD signal
	P30/RXD0	6	GPIO/UART0 receive RXD signal
	GND	7,13,15,17 19	Ground
	TXD0_232	8	UART0 TXD signal on RS232 voltage level
	RXD0_232	9	UART0 TXD signal on RS232 voltage level
	PC4/TERR#	10	GPIO/Optional JTAG status(TERR)
	P35/C1	11	GPIO/Counter1 input
	VCC2	12	5V power
	P17/AD7	14	GPIO/SPI slave select/ADC channel 7
	P15/AD5	16	GPIO/SPI receive/ADC channel 5
	P13/AD3	18	GPIO/UART1 or IrDA transmit/ADC channel 3
	RESET#	20	System reset signal

CN5	ALE	1	Address latch signal
	PD2	2	GPIO/PLD input and output
	PB0	13	GPIO/PLD IO/Address Latch output
	PB1	3,12	GPIO/PLD IO/Address Latch output
	PB2	4,11	GPIO/PLD IO/Address Latch output
	PB3	5,10	GPIO/PLD IO/Address Latch output
	PB4	6	GPIO/PLD IO/Address Latch output
	PB5	7	GPIO/PLD IO/Address Latch output
	PB6	8	GPIO/PLD IO/Address Latch output
	PB7	9	GPIO/PLD IO/Address Latch output
	VCC2	14	5V power
	P16/ADC6	15	GPIO/SPI transmit/ADC channel 6
	VCC3	16,18	3.3V power
	P14/ADC4	17	GPIO/SPI clock output/ADC channel 4
	P12/ADC2	19	GPIO/UART1 or IrDA receive/ADC channel 2
	P10/ADC0	20	GPIO/Timer 2 counter input/ADC channel 0

3.1.4 ED3K4 Top connection capabilities

Various external connectivity is provided based on 100-pin connector on ED3K4, including 7 channels of ADC, 6 channels of PWM/SERVO output, 3 channels of Timing capture, SRAM backup power input, UART1 RS232 level, UART0 digital level, POWER-DOWN input, External battery, External clock, I2C and External RESET. All possible top connection capabilities have been listed in following *Table 4*.

Table 4. ED3K4 Top connection capabilities

Capabilities	Signals name	Headers
SRAM backup power	PC2/VSTBY	CON2.1
	GND	CON2.2
PWM/SERVO OUTPUT1	GND	CON1.3
	VCC1	CON2.3
	MCU_SPI_TXD	CON3.3
PWM/SERVO OUTPUT2	GND	CON1.4
	VCC1	CON2.4
	MCU_SPI_RXD	CON3.4
PWM/SERVO OUTPUT3	GND	CON1.5
	VCC1	CON2.5
	MCU_SPI_CLK	CON3.5
PWM/SERVO OUTPUT4	GND	CON1.6
	VCC1	CON2.6
	P42/TCM2	CON3.6

PWM/SERVO OUTPUT5	GND	CON1.7
	VCC1	CON2.7
	P41/TCM1	CON3.7
PWM/SERVO OUTPUT6	GND	CON1.8
	VCC1	CON2.8
	P40/TCM0	CON3.8
TIMING CAPTURE 1	GND	CON1.9
	PA7	CON2.9
	P32/INT0	CON3.9
TIMING CAPTURE 2	GND	CON1.10
	PA6	CON2.10
	P33/INT1	CON3.10
TIMING CAPTURE 3	GND	CON1.11
	PA5	CON2.11
	P11/T2X	CON3.11
UART1 RS232 level	TXD1_232	CON3.13
	RXD1_232	CON3.14
POWER-DOWN	PWR_DOWN	CON2.17
	GND	CON3.17
EXTERNAL BATTERY CONNECTION	VBATT	CON2.18
	GND	CON2.19
EXTERNAL CLOCK INPUT	EXT_CLK	CON2.20
	GND	CON2.19
I2C BUS WITH GND+POWER	GND	CON3.17
	P36/SDA	CON3.18
	P37/SCL	CON3.19
	VCC3	CON3.20
UART0 DIGITAL LEVEL	P31/TXD0	CON4.5
	P30/RXD0	CON4.6
	GND	CON4.7
ADC channel 1	P11/T2X	CON3.11
	GND	CON3.12
ADC channel 2	P12/ADC2	CON5.19
	GND	CON4.19
ADC channel 3	P13/ADC3	CON4.18
	GND	CON4.19
ADC channel 4	P14/ADC4	CON5.17
	GND	CON4.17
ADC channel 5	P15/ADC5	CON4.16
	GND	CON4.17
ADC channel 6	P16/ADC6	CON5.15
	GND	CON4.15

ADC channel 7	P17/ADC7	CON4.14
	GND	CON4.13
EXTERNAL RESET	RESET#	CON4.20
	GND	CON4.19

3.1.5 LEDs on ED3K4

There are 7 LEDs to indicate the work status on ED3K4 board. D5 and D8 are driven by Power management chips. LD1, LD2 and LD3 are used to indicate the work status of the embedded Rlink. D2 is used to indicate the JTAG operation. D6 is a user LED that can be driven by uPSD PD1. All the LEDs D5, D6, D8, LD1, LD2 and LD3 are located on the area near by the eRlink USB port. D2 is located on the area near the POWER connector. Please find the detailed information in *Table 5*.

Table 5. LED description

LED	Color	Usage
D2	red	JTAG operation indicator LED
D5	red	Power indicator LED
D8	red	Low battery indicator LED
LD1	green	eRlink Power indicator LED
LD2	red	eRlink BUSY indicator LED
LD3	green	eRlink RUN indicator LED
D6	red	User LED that can be driven by uPSD3434E on board

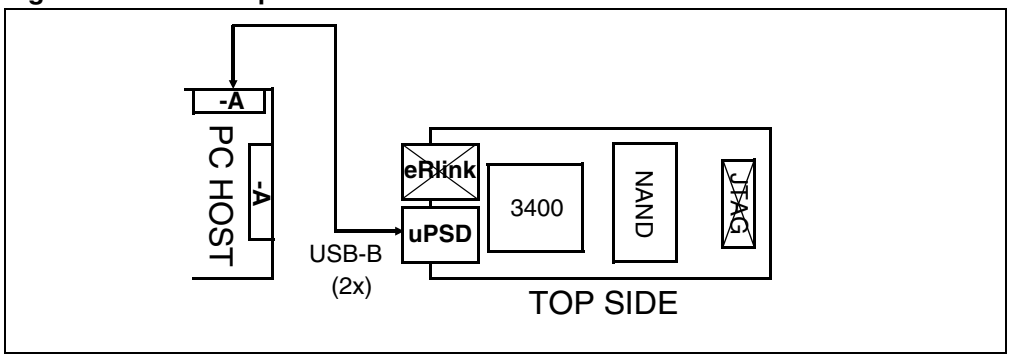
3.2 ED3K4 Operation Mode

The ED3K4 is a versatile uPSD3400 module with 5 user operation modes. You may treat it as a uPSD3400 user target board, standalone debug tools RLINK or an integrated uPSD3400 development platform with embedded SW evaluation capability depending on the relative configuration and usage. The 5 operation modes will be introduced in the following chapter one by one.

3.2.1 Operation Mode 1: USB Mass Storage Mode

The ED3K4 module may be used as a low speed USB device with file storage function on operation mode1. Connected to PC with WinXP via a USB cable, it can be used to download and upload files to or from the ED3K4 module.

Figure 5. ED3K4 operation mode 1 connection



Hardware connection on Mode 1

Please refer to *Figure 5* for the connection on operation mode 1.

Configuration of jumpers on Mode 1

Please refer to *Table 6* for detailed information about jumper configuration on operation mode 1.

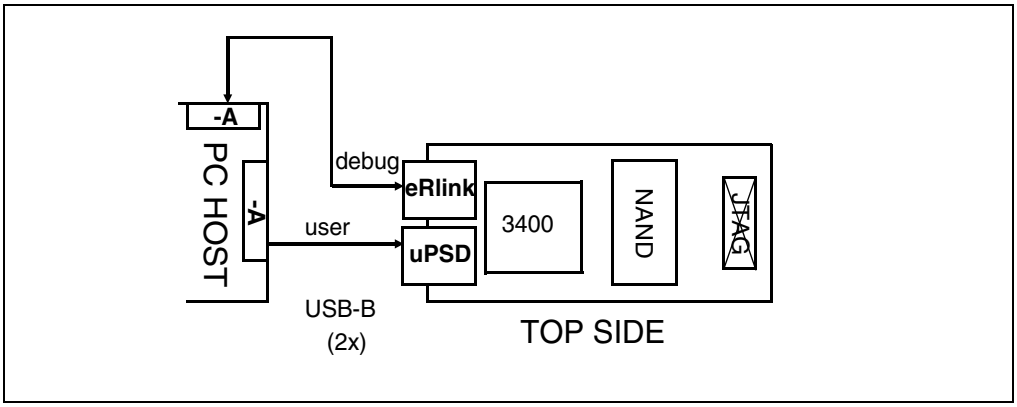
Table 6. Jumper configuration on Mode 1

Jumper	Status	Jumper	Status	Jumper	Status
JP1	closed	JP5	1<->2	JP9	closed
JP2	open	JP6	closed	JP10	closed
JP3	closed	JP7	1<->2	JP11	open
JP4	1<->2	JP8	closed	JP12	1<->3;2<->4

3.2.2 Operation Mode 2: uPSD+E-RLINK Mode

The ED3K4 module may be used as integrated uPSD3400 development platform with embedded RLINK on operation mode2. You can build the small uPSD3400 platform by simply connecting the ED3K4 to a PC with RIDE via a USB cable.

Figure 6. ED3K4 operation mode 2 connection



Hardware connection on Mode 2

Please refer to *Figure 6* for the connection on operation mode 2.

Configuration of jumpers on Mode 2

Please refer to *Table 7* for detailed information about jumper configuration on operation mode 2.

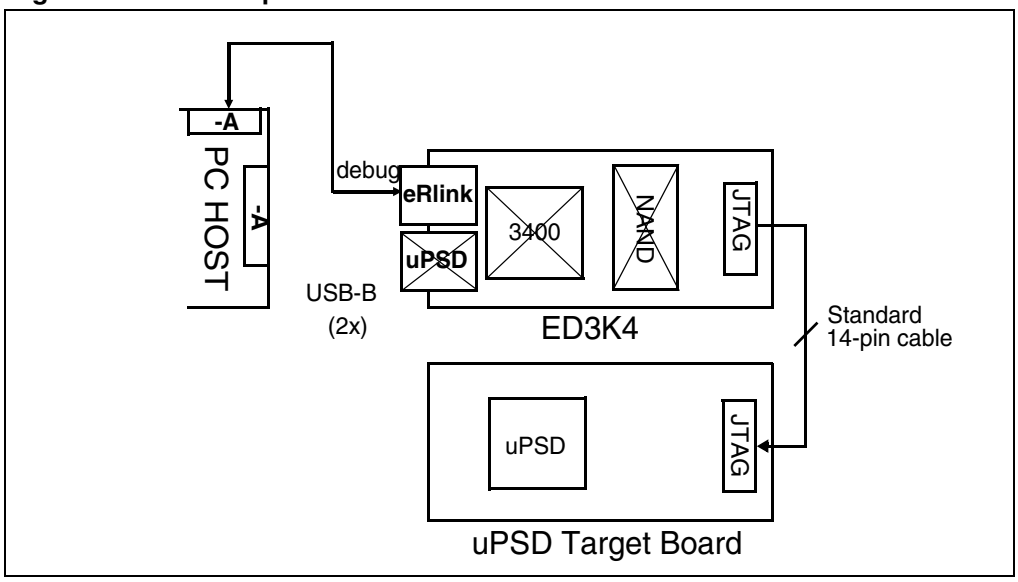
Table 7. Jumper configuration on Mode 2

Jumper	Status	Jumper	Status	Jumper	Status
JP1	closed	JP5	2<->3	JP9	closed
JP2	open	JP6	closed	JP10	closed
JP3	closed	JP7	1<->2	JP11	open
JP4	1<->2	JP8	closed	JP12	1<->3;2<->4

3.2.3 Operation Mode 3: Stand-alone RLINK mode

The ED3K4 module may be used as a stand-alone uPSD debug tool like RLINK on operation mode3. Only the embedded RLINK is active on ED3K4 board on this operation mode.

Figure 7. ED3K4 operation mode 3 connection



Hardware connection on Mode 3

Please refer to *Figure 7* for the connection on operation mode 3.

Configuration of jumpers on Mode 3

Please refer to *Table 8* for detailed information about jumper configuration on operation mode 3.

Table 8. Jumper configuration on Mode 3

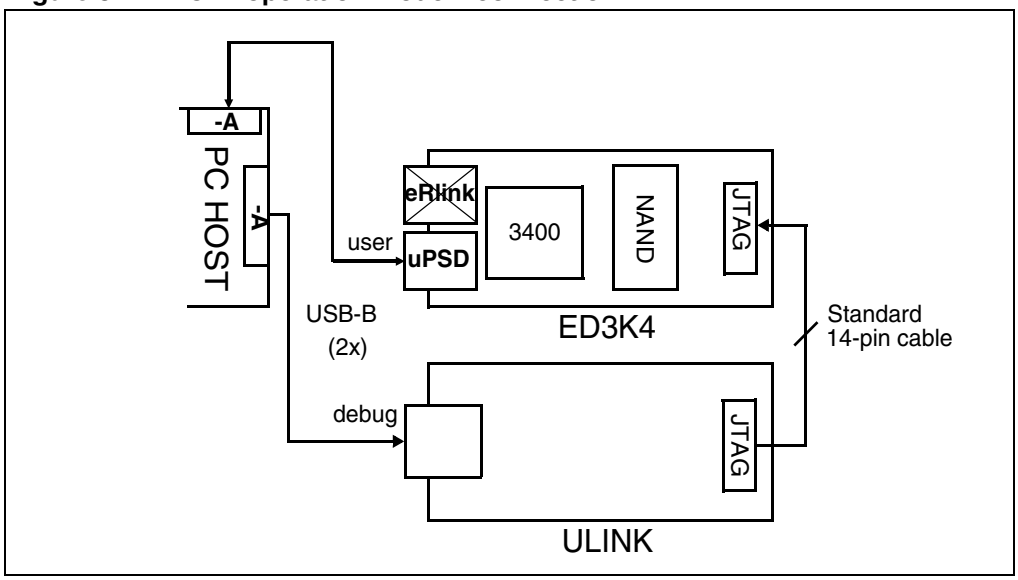
Jumper	Status	Jumper	Status	Jumper	Status
JP1	closed	JP5	1<->2	JP9	closed

JP2	open	JP6	closed	JP10	open
JP3	closed	JP7	1<->2	JP11	open
JP4	open	JP8	closed	JP12	1<->3;2<->4

3.2.4 Operation Mode 4: uPSD+ULINK mode

The ED3K4 module may be treated as a uPSD target board on operation mode4. The embedded RLINK on board is disabled in this mode. You may connect ED3K4 with another JTAG-based uPSD debug tools like ULINK from Keil in this mode.

Figure 8. ED3K4 operation mode 4 connection



Hardware connection on Mode 4

Please refer to *Figure 8* for the connection on operation mode 4.

Configuration of jumpers on Mode 4

Please refer to *Table 9* for detailed information about jumper configuration on operation mode 4.

Table 9. Jumper configuration on Mode 4

Jumper	Status	Jumper	Status	Jumper	Status
JP1	closed	JP5	1<->2	JP9	open
JP2	open	JP6	closed	JP10	closed
JP3	closed	JP7	1<->2	JP11	open
JP4	1<->2	JP8	closed	JP12	1<->3;2<->4

3.2.5 Operation Mode 5: ED3K4+DK3400 Motherboard mode

The ED3K4 module is capable of working together with the DK3400 motherboard in operation mode 5. The dot-matrix LCD, RS232 connector and PS/2 Keyboard are available for use in this operation mode. The default DK3400 will be delivered with mode 5. You are allowed to program and debug DK3400 using alternative JTAG debug tools, embedded Rlink or external ULINK on mode 5. Please make sure that the jumper configuration of JP9 and JP10 is compatible with requirement in mode 2 when you select eRlink as debug tools. Please also make sure that the jumper configuration of JP9 and JP10 is compatible with requirement in mode 4 when you select external ULINK as debug tools.

Hardware connection on Mode 5

Just plug ED3K4 module in the ED3Kx socket on DK3400 motherboard.

Configuration of jumpers on Mode 5

Please refer to *Table 10* for detailed information about jumper configuration on operation mode 5.

Table 10. Jumper configuration on Mode 5

Jumper	Status	Jumper	Status	Jumper	Status
JP1	closed	JP5	open	JP9	closed
JP2	open	JP6	open	JP10	closed
JP3	closed	JP7	1<->2	JP11	open
JP4	1<->2	JP8	closed	JP12	1<->3;2<->4

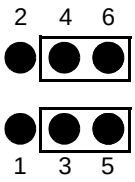
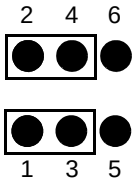
4 DK3400 Motherboard Hardware Architecture

The DK3400 motherboard can be used as a base board for both the uPSD module ED3K4 and ED3K3. The power supply, LCD, RS232 interface and PS/2 Keyboard interface are available on this board.

4.1 Jumper description

The jumper definitions on the DK3400 motherboard are listed in *Table 11*.

Table 11. Description of jumpers on DK3400 motherboard

Jumper	Description
JP1	JP1 is used to select which UART port is connected to RS232 connector on DK3400 motherboard. UART0 is connected to RS232 connector when JP1 is set as following:  UART1 is connected to RS232 connector when JP1 is set as following:  Default status: JP1.3 connected to JP1.5; JP1.4connected to JP1.6.

4.2 Connector description

The connector definitions on the DK3400 motherboard are listed in *Table 12*.

Table 12. Description of connectors on DK3400 motherboard

Connector	Description
CN0	9V power jack.
CN1,2,3,4 and 5	Connectors for ED3Kx module
CN6	RS232 connector (female)
CN7	PS/2 standard Keyboard connector
DKMMX_CON1	Connector for DKMMX board
DKMMX_CON2	Connector for DKMMX board
DKMMX_CON3	Connector for DKMMX board

5 Getting Started With DK3400

The DK3400 is delivered in default operation mode 5 with the RTC demonstration application.

Please follow the steps below to get started using the DK3400:

Check with Jumper configuration

Please check the jumper configuration to guarantee that all jumper status are the same as those listed in *Table 10* (ED3K4 operation mode 5).

Connecting DK3400 board for RTC demo

1. Connect the AC adapter to the DK3400 board. The DK3400 AC adapter will work on either 110V or 220V, and contains several different plug adapters to fit popular European AC outlets. Please set up your AC adapter to fit your AC plug type and plug in the AC adapter. Then plug the small power plug into the DK3400 9V DC input.
2. Connect a PS/2 standard Keyboard to PS/2 connector on DK3400 motherboard.

Step 3 - Try Your DK3400 Board with RTC demo.

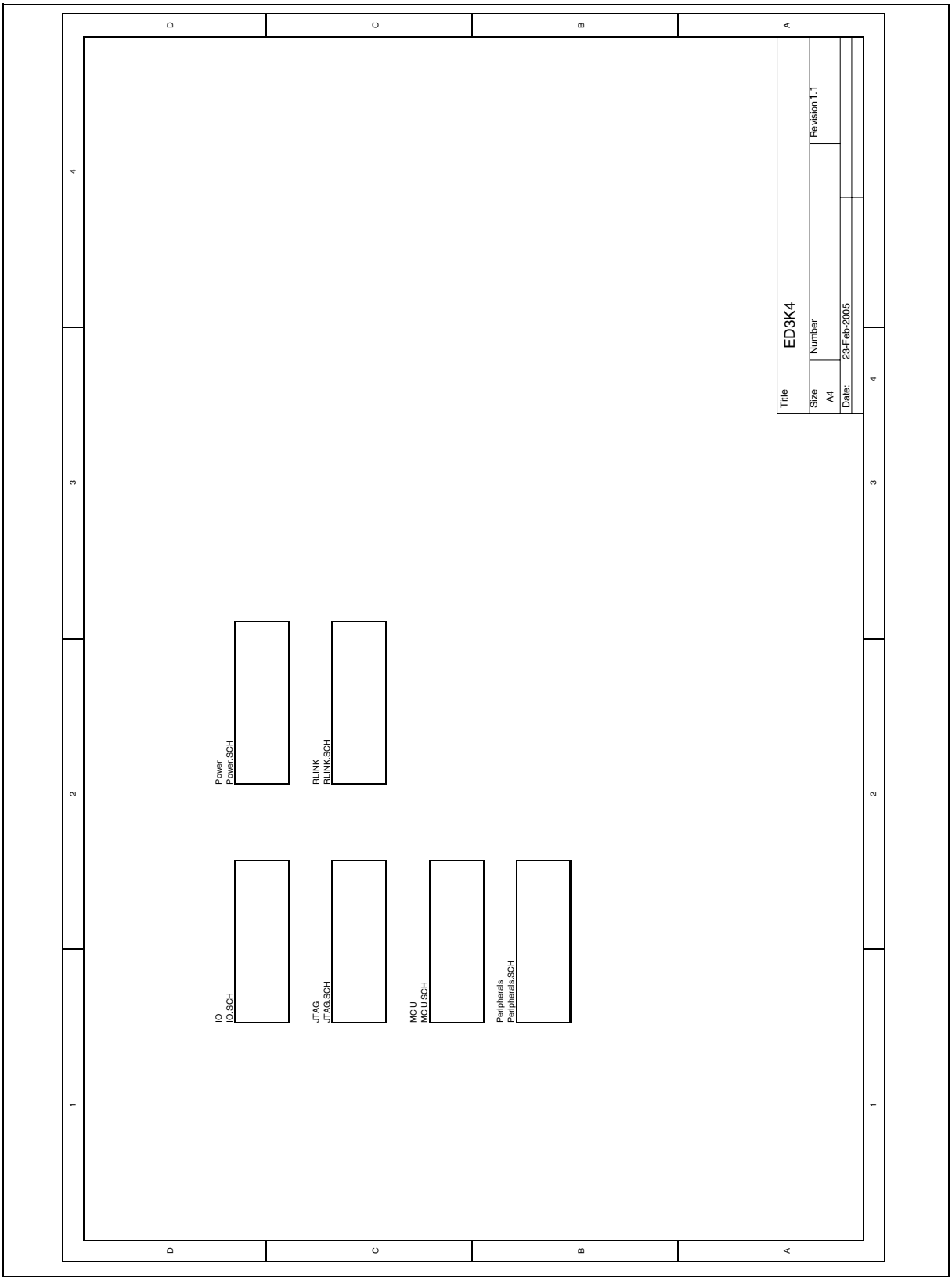
Turn DK3400 on. Your DK3400 board will boot from RTC demo application.

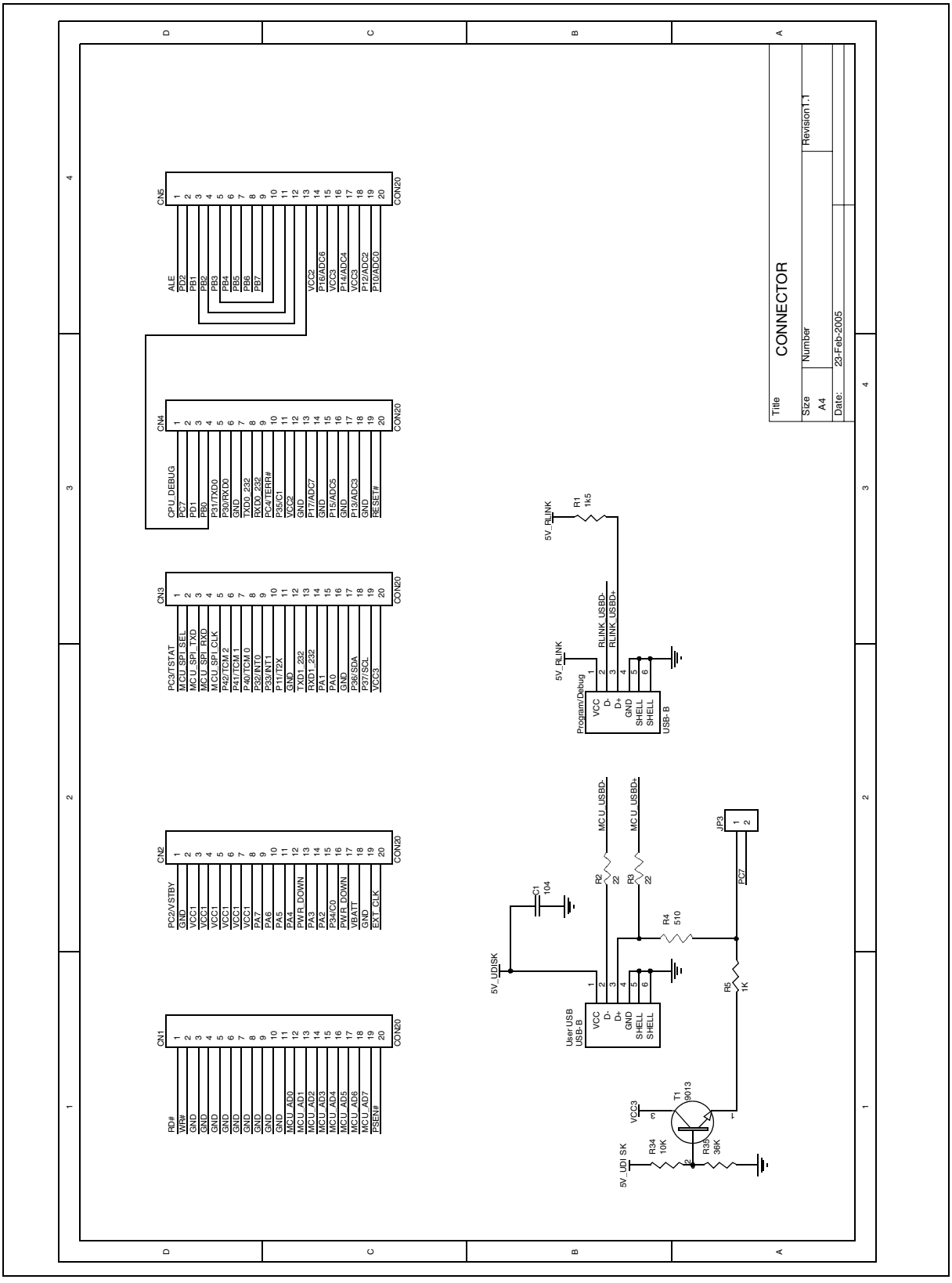
You should see the DK3400 RTC demo running in the LCD window. The RTC time can be updated by pressing keys “up”, “down”, “left”, “right” and “enter” on the Keyboard.

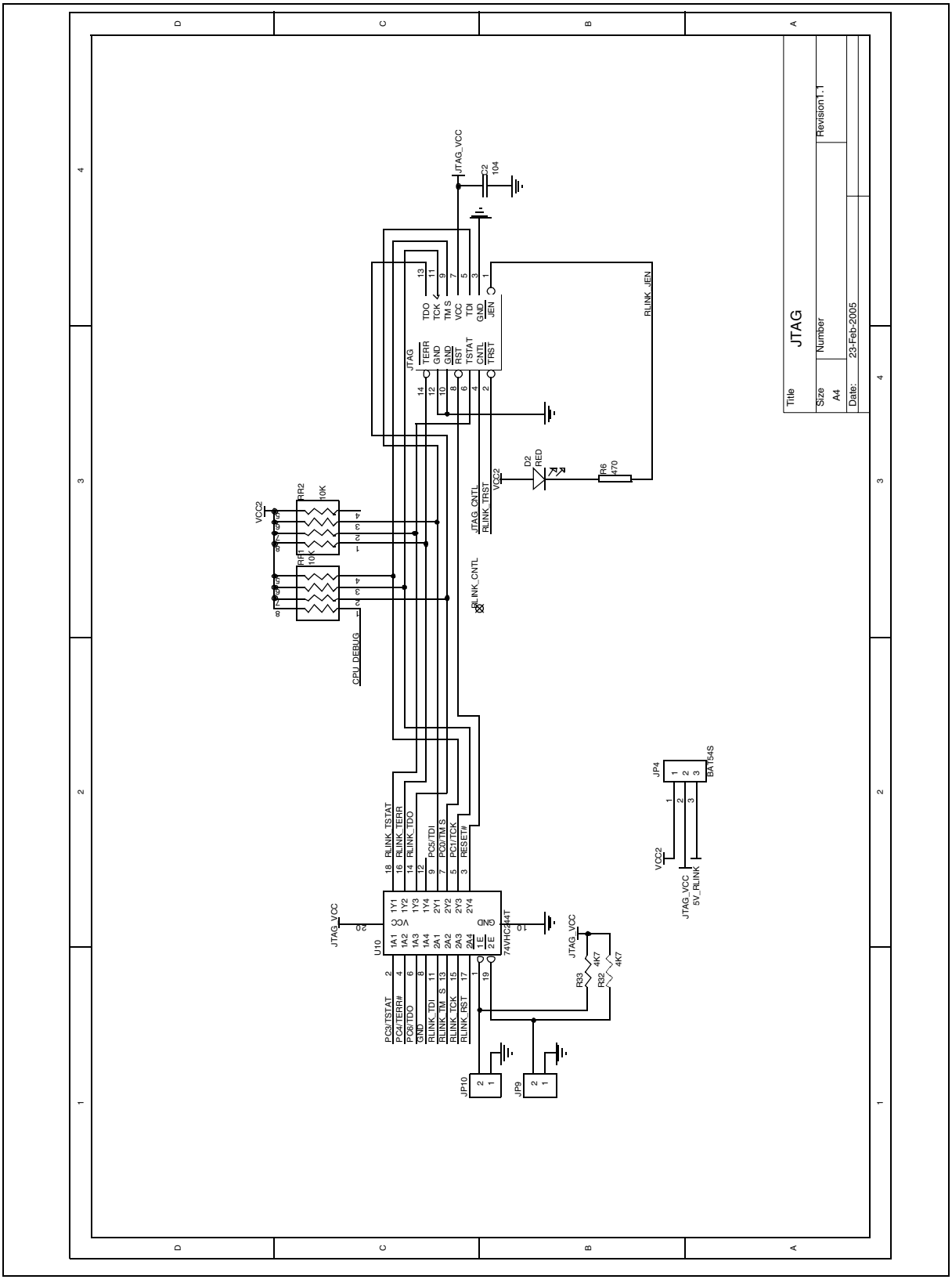
Additional Information

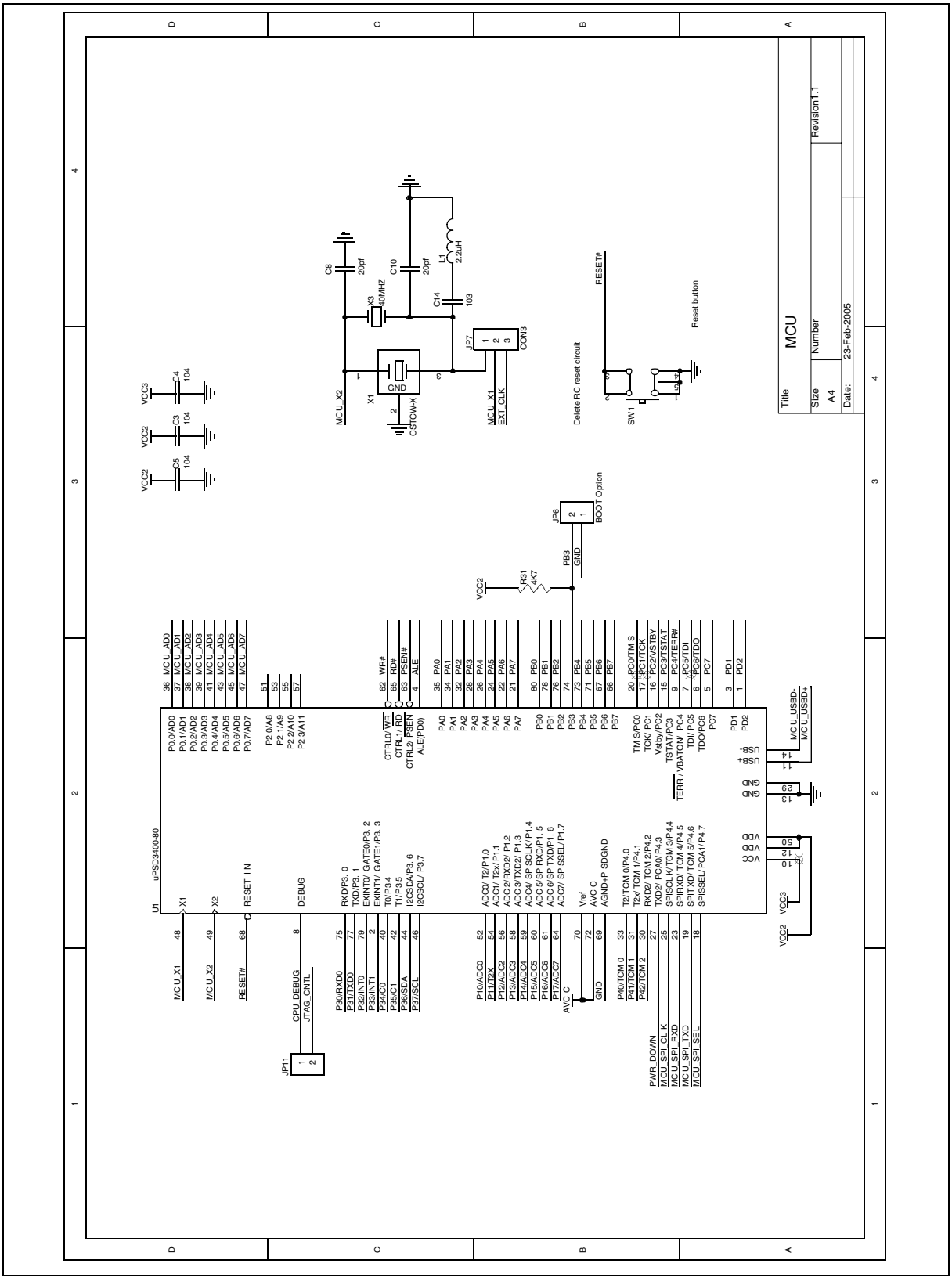
The uPSD3400 series design guide application notes for DK3400 using RIDE or KEIL's software tools are available for download from the ST website:
http://www.st.com/psm

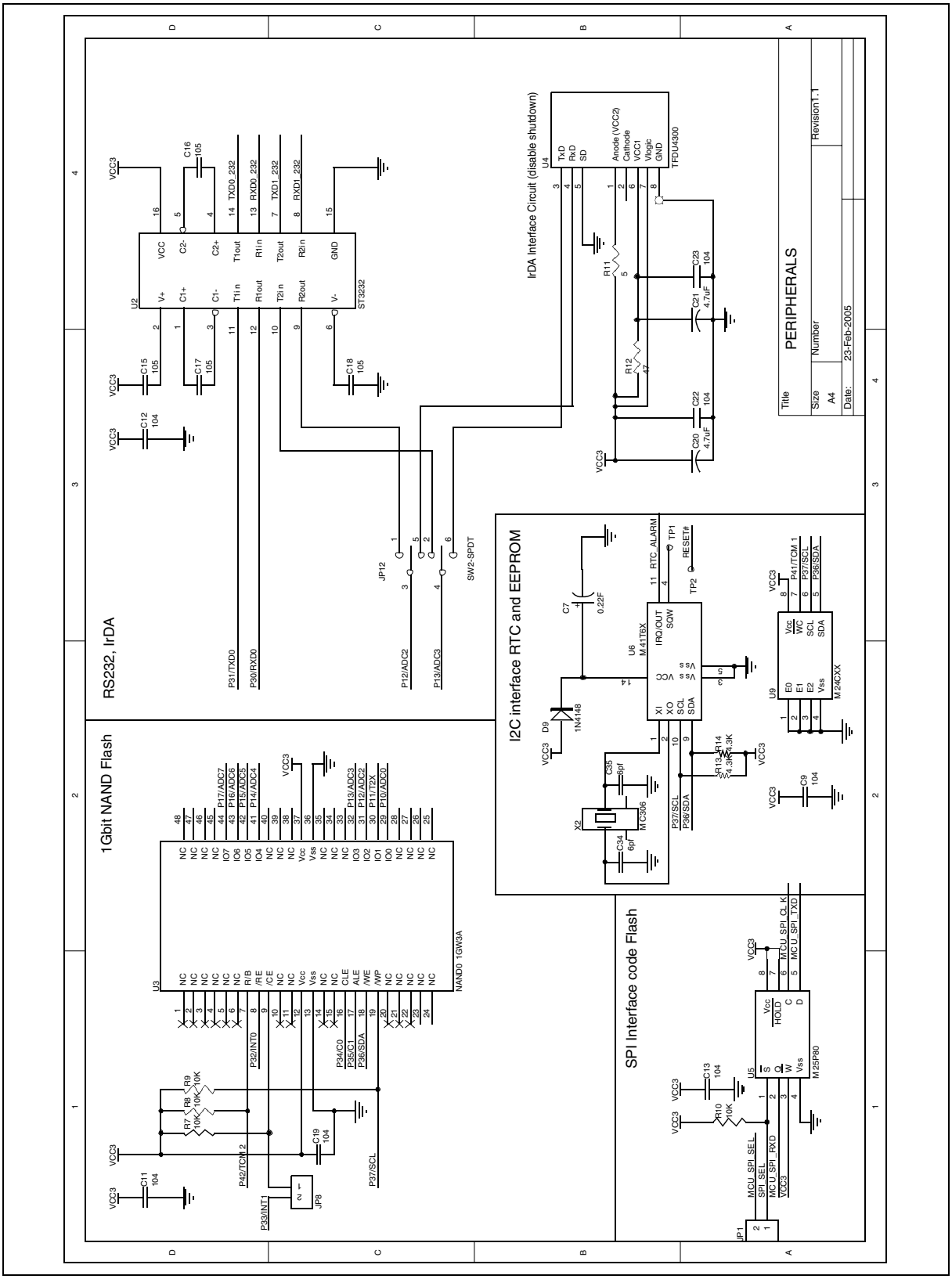
Appendix A ED3K4 Schematic

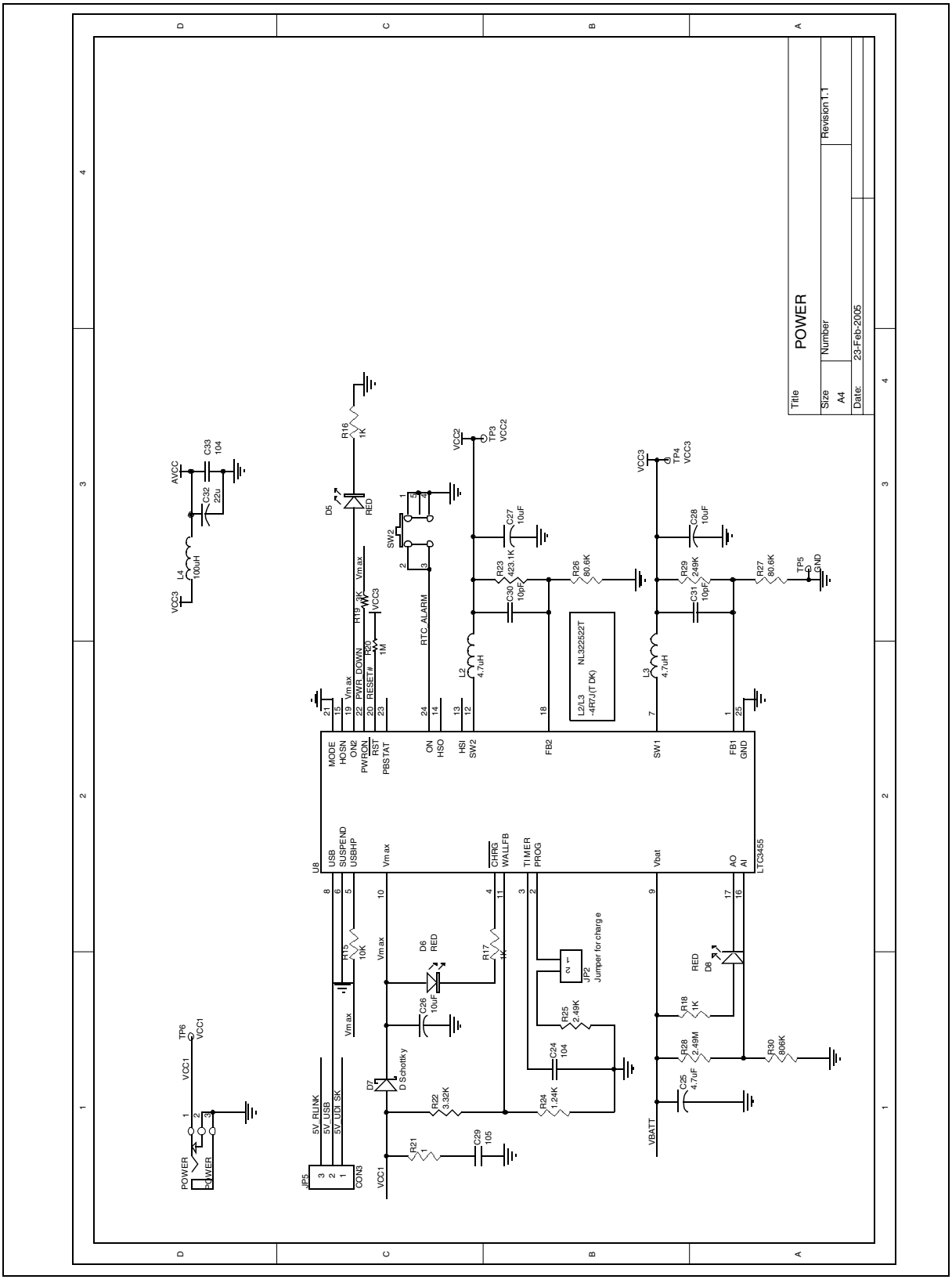


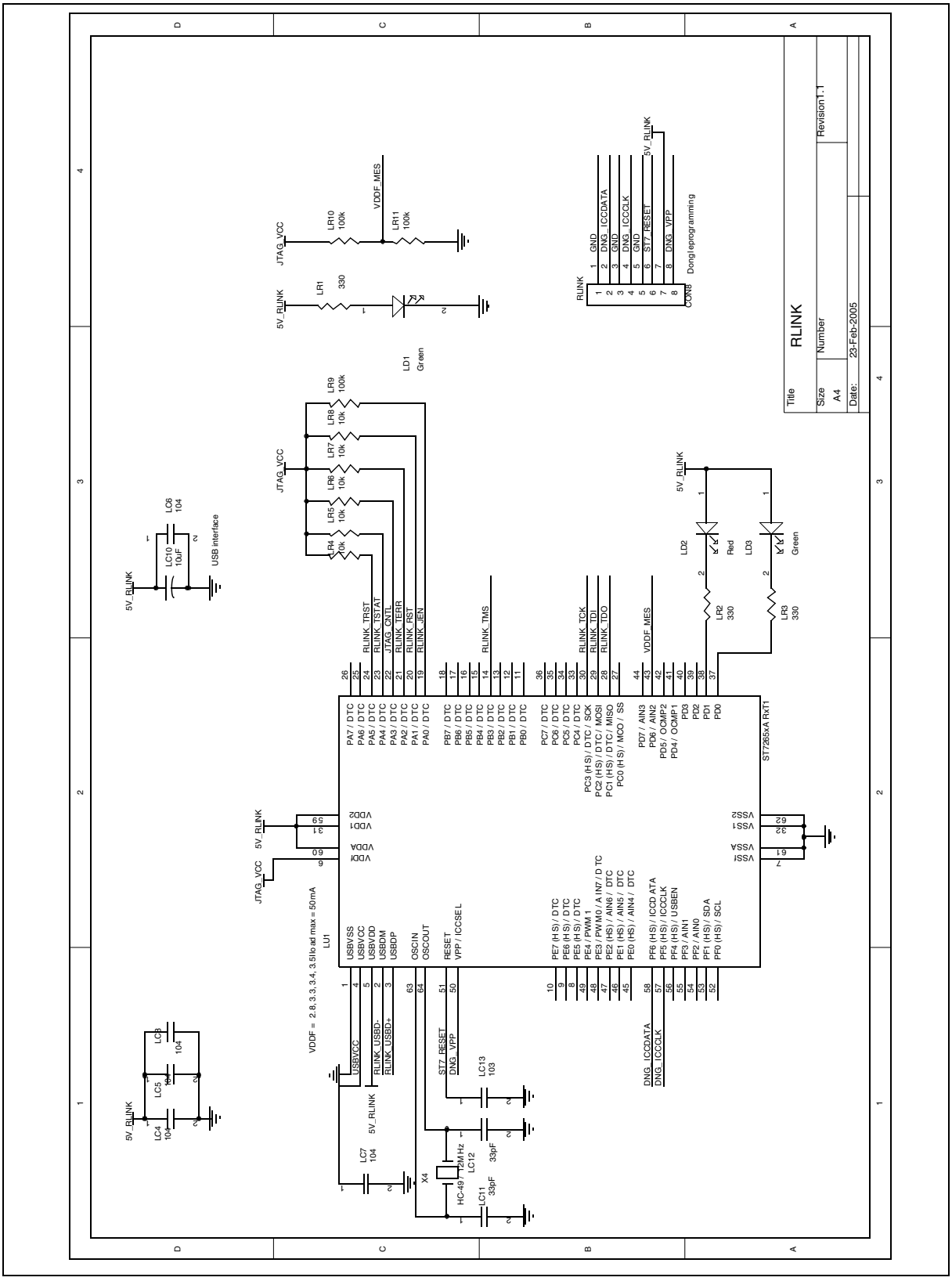

CONNECTOR
Revision 1.1
Size A4
Number
Date: 29-Feb-2005
CN5
CON20
ALE
PD2
PB1
PB2
PB3
PB4
PB5
PB6
PB7
VCC2
P16/ADC6
VCC3
P14/ADC4
VCC3
P12/ADC2
P10/ADC0
CN4
CON20
CPU_DEBUG
PC7
PD1
PB0
P31/TXD0
P30/RX0
GND
TXD0_232
RXD0_232
PC4/TERR#
P35/CT1
VCC2
GND
P17/ADC7
GND
P15/ADC5
GND
P13/ADC3
GND
RESET#
CN3
CON20
PC3/TSTAT
MCU_SPI_SEL
MCU_SPI_TXD
MCU_SPI_RXD
MCU_SPI_CLK
P42/TCM2
P41/TCM1
P40/TCM0
P29/INT0
P28/INT1
P11/T2X
GND
TXD1_232
RXD1_232
PA1
PA0
GND
P36/SDA
P37/SCL
VCC3
CN2
CON20
PC2/VSTBY
GND
VCC1
VCC1
VCC1
VCC1
VCC1
PA7
PA6
PA5
PA4
PWR_DOWN
PA3
PA2
P34/C0
PWR_DOWN
VBATT
GND
EXT_CLK
CN1
CON20
RD#
WR#
GND
GND
GND
GND
GND
GND
GND
MCU_AD0
MCU_AD1
MCU_AD2
MCU_AD3
MCU_AD4
MCU_AD5
MCU_AD6
MCU_AD7
PSEN#
5V_RLINK
R1
1k5
RLINK_USBD-
RLINK_USBD+
5V_RLINK
Program/Debug
VCC
D-
D+
GND
SHELL
SHELL
USB- B
MCU_USBD-
MCU_USBD+
JP3
PC7
C1
104
R2
22
R3
22
R4
510
5V_UDISK
R5
1K
User USB
USB-B
VCC
D-
D+
GND
SHELL
SHELL
VCC3
T1
9013
5V_UDI SK
R34
10K
R35
36K


JTAG
Title
Size
A4
Number
Revision1.1
Date:
23-Feb-2005
JTAG_VCC
C22
104
JTAG
TERR
GND
GND
RST
TSTAT
CNTL
TRST
TDO
TCK
TM S
VCC
TDI
GND
JEN
RLINK_JEN
D2
RED
R6
470
VCC2
JTAG_CNTL
RLINK_TRST
RLINK_CNTL
RR2
10K
RR1
10K
CPU_DEBUG
RLINK_TSTAT
RLINK_TERR
RLINK_TDO
PC5/TDI
PC0/TMS
PC1/TCK
RESET#
U10
74VHC244T
JTAG_VCC
R33
4K7
R32
4K7
JP4
BAT54S
VCC2
JTAG_VCC
5V_RLINK
JP10
JP9
PC2/TSTAT
PC4/TERR#
PC6/TDO
GND
RLINK_TDI
RLINK_TM_S
RLINK_TCK
RLINK_RST

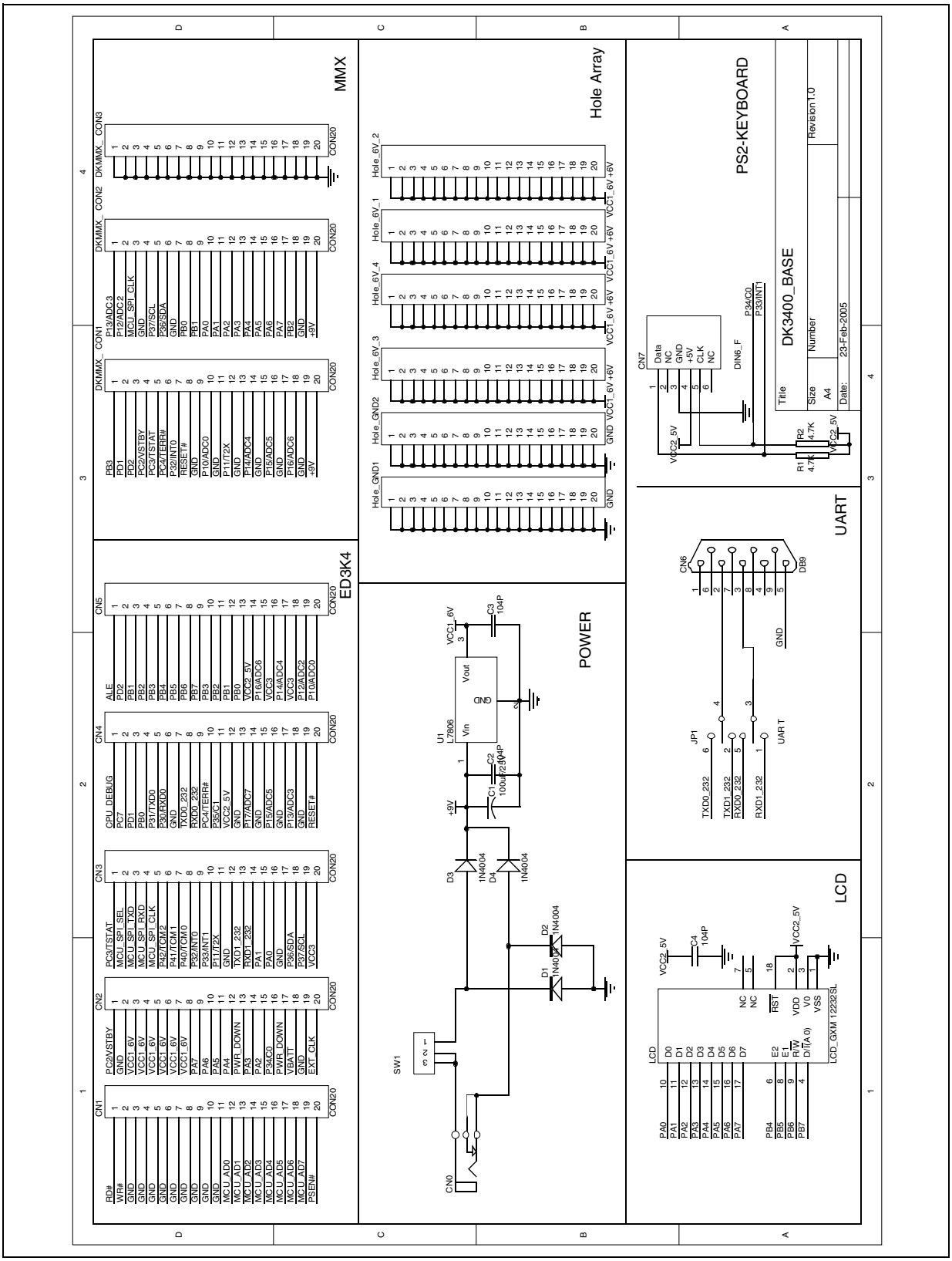

Title MCU
Size Number Revision1.1
A4
Date: 23-Feb-2005
U1 uPSD3400-80
MCU_X1
MCU_X2
RESET#
DEBUG
CPU_DEBUG
JTAG_CNTL
JP11
X1
X2
RESET_I N
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
P0.4/AD4
P0.5/AD5
P0.6/AD6
P0.7/AD7
P2.0/A8
P2.1/A9
P2.2/A10
P2.3/A11
MCU_AD0
MCU_AD1
MCU_AD2
MCU_AD3
MCU_AD4
MCU_AD5
MCU_AD6
MCU_AD7
WR#
RD#
PSEN#
ALE
CTRL0/ WR#
CTRL1/ RD#
CTRL2/ PSEN#
ALE(P D0)
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
JP6
BOOT Option
PB3
GND
VCC2
R31
4K7
TM S/PC0
TCK/ PC1
Vstby/PC2
TSTAT/PC3
TERR/ VBATON/ PC4
TDI/ PC5
TDO/PC6
PC7
PD1
PD2
USB-
USB+
MCU_USBD-
MCU_USBD+
GND
VDD
VCC
VCC3
VCC2
P30/RXD/P3. 0
P31/TXD/P3. 1
P32/INT0/P3. 2
P33/INT1/P3. 3
P34/C0
P35/C1
P36/SDA
P37/SCL
P10/ADC0
P11/T2X
P12/ADC2
P13/ADC3
P14/ADC4
P15/ADC5
P16/ADC6
P17/ADC7
AVC C
GND
P40/TCM 0/P4.0
P41/TCM 1/P4.1
P42/TCM 2/P4.2
PWR_DOWN
MCU_SPI_CLK
MCU_SPI_RXD
MCU_SPI_TXD
MCU_SPI_SEL
RXD/P3. 0
TXD/P3. 1
EXINT0/ GATE0/P3. 2
EXINT1/ GATE1/P3. 3
T0/P3.4
T1/P3.5
I2CSDA/P3. 6
I2CSCL/ P3.7
ADC0/ T2/P1.0
ADC1/ T2x/P1.1
ADC 2/RXD2/ P1.2
ADC 3/TXD2/ P1.3
ADC4/ SPISCLK/P1.4
ADC 5/SPIRXD/P1. 5
ADC 6/SPITXD/P1. 6
ADC7/ SPISSEL/P1.7
Vref
AVC C
AGND-P SD/GND
T2/TCM 0/P4.0
T2x/ TCM 1/P4.1
RXD2/ TCM 2/P4.2
TXD2/ PCA0/ P4.3
SPISCL K/TCM 3/P4.4
SPIRXD/ TCM 4/P4.5
SPIT XD/TCM 5/P4.6
SPISSEL/ PCA1/ P4.7
C8 20pf
C10 20pf
L1 2.2uH
C14 103
X3 40MHZ
X1
GND
CSTCW-X
MCU_X2
MCU_X1
EXT CLK
JP7
CON3
C4 104
C3 104
C5 104
VCC3
VCC2
VCC2
Delete RC reset circuit
RESET#
SW1
Reset button


RS232, IrDA
IrDA Interface Circuit (disable shutdown)
I2C interface RTC and EEPROM
1Gbit NAND Flash
SPI Interface code Flash
PERIPHERALS
Revision1.1
23-Feb-2005
ST3232
TFDU4300
M41T6X
M24CXX
M25P80
SW2-SPDT
NAND0 1GW3A


POWER
Title
Size
A4
Number
Revision 1.1
Date:
23-Feb-2005
LTC3455
U8
MODE
HOSN
ON2
PWRON
RST
PBSTAT
ON
HSO
HSI
SW2
FB2
SW1
FB1
GND
USB
SUSPEND
USBHP
Vmax
CHRG
WALLFB
TIMER
PROG
Vbat
AO
AI
L2/L3
-4R7J(TDK)
NL322522T
L2
4.7uH
L3
4.7uH
L4
100uH
RTC_ALARM
PWR_DOWN
RESET#
VCC3
VCC2
VCC1
AVCC
VBATT
Jumper for charge
JP2
JP5
CON3
5V_RUNK
5V_USB
5V_UDI_SK
POWER
D5
D6
D7
D8
RED
D Schottky
SW2
TP3
TP4
TP5
TP6
GND


RLINK
Title
Size
A4
Number
Revision1.1
Date:
23-Feb-2005
ST7265xA RxT1
LU1
LD1
Green
LD2
Red
LD3
Green
USB interface
Dongleprogramming
RLINK_TRST
RLINK_TSTAT
JTAG_ONTI
RLINK_TERR
RLINK_RST
RLINK_JEN
RLINK_TMS
RLINK_TCK
RLINK_TDI
RLINK_TDO
VDDF_MES
RLINK_USBD-
RLINK_USBD+
ST7_RESET
DNG_VPP
DNG_ICCDATA
DNG_ICCCLK
5V_RLINK
JTAG_VCC
VDDF = 2.8, 3.3, 3.4, 3.5 to add max = 50mA

Appendix B DK3400 Motherboard Schematic



6 Revision History

Date	Revision	Changes
01-Mar-2005	1	First Release

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ask.memory@st.com (*for general enquiries*)

Please remember to include your name, company, location, telephone number and fax number.

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